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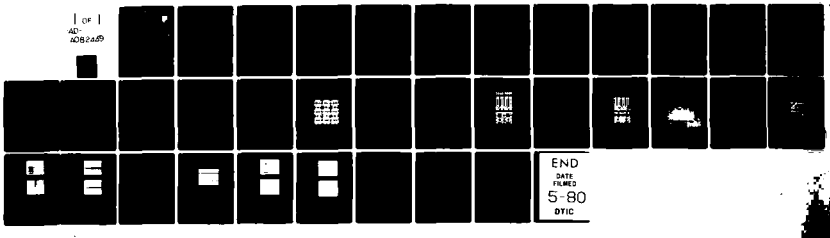

RADC-TR-79-294
Interim Report
December 1979

AN ANALOG CCD REFORMATTING MEMORY EMPLOYING TWO-DIMENSION CHARGE TRANSFER

Texas Instruments, Incorporated

Robert J. Kansy

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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APPROVED: Virgil E Vickers

VIRGIL E. VICKERS
Project Engineer

APPROVED: Robert M Barrett

ROBERT M. BARRETT, Director
Solid State Sciences Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An analog CCD reformatting memory has been designed and fabricated using an N-channel double level polysilicon gate process. This unique CCD structure employs two-dimensional charge transfer cells in a 32x32 element array which is accessed by means of integrated CCD demultiplexer and multiplexer structures resulting in greater dynamic range than observed in previous line-addressed designs. The design and operation of this structure are discussed, and examples of application in signal processor architectures are described.

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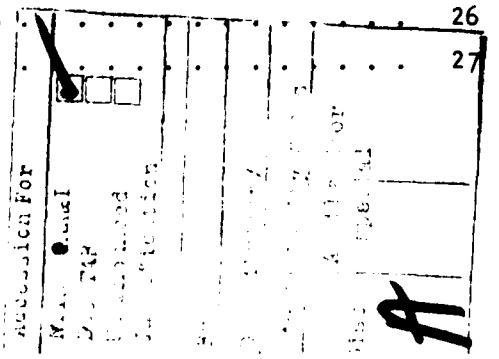


I. INTRODUCTION

Advancements in charge-coupled device technology have resulted in the addition of a number of new components for analog signal processing applications. The most promising developments in this field are the integrated chirp Z-transform (CZT)[1] and the digital-analog correlator,[2] both of which capitalize on the tremendous effective computational power of analog transversal filters in order to accomplish complex signal processing fuctions with modest volume, weight and power dissipation. These devices can be thought of as linear operators which transform a fixed length input record V into an output record U of identical length according to U=LV. In the case of the chirp Z-transorm, L corresponds to the discrete Fourier transform operator via the chirp Z algorithm, while in the digital-analog correlator L corresponds to a programmable scalar product operator.

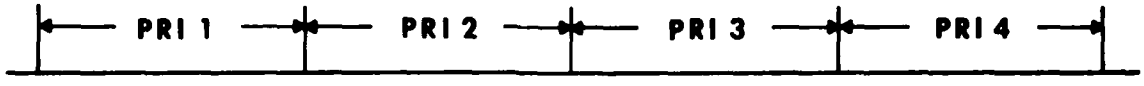
Unfortunately, in a number of potentially interesting applications the input data sequence does not occur in the form of consecutive, fixed length input records. A particularly illustrative example is the case in which it is desired to utilize the CZT processor to accomplish doppler resolution of the returns in a pulsed radar system. The situation is illustrated in Figure 1a which shows the radar video in each transmitter pulse repetition inteval (PRI) subdivided into range bins which are dictated by the range resolution of the radar circuitry.

In order to accomplish the doppler processing, the returns in each range bin must be analyzed over a number of PRIs dictated by the number of points in the transform. Use of an integrated CZT processor in this application requires that the input record be sequential in PRIs, whereas the radar video is sequential in range bins. Figures 1b through 1e illustrate the problem.

The radar video shown in Figure 1b is low pass filtered and sampled at a rate commensurate with the range resolution resulting in Figure 1c. For illustrative purposes a constant amplitude return (stationary target) is shown in range bin 1 and a time varying return (moving target) is shown in range bin 3. The serial video consists of 4 records, each of length 8 which are grouped in a 4x8 matrix format in Figure 1d. The rows correspond to pulse intervals and columns to range bins within each interval. If we consider Figure 1d as representing the contents of a 4x8 memory array into which the sampled video was loaded on a row-by-row basis, then it can be seen that the desired reformatting operation consists in reading the contents of the memory column-by-column. This results in 8 records, each 4 samples in length and each sequential in pulse interval, as required for doppler processing and shown in Figure 1e.

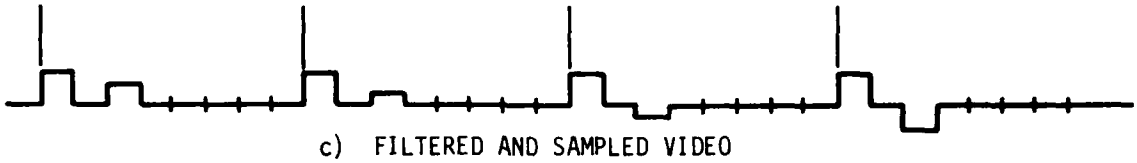
It can be shown that the minimum number of storage locations required to accomplish the reformatting operation on M records of length N is (N-1)(M-1). However, the access and transfer control requirements for a CCD memory of this type are quite complex. Considerable simplification results from the use of a MxN array as illustrated in Figure 1, in that all access and transfer operations can be made to occur either sequentially or in parallel.

The configuration of the hypothetical doppler processor subsystem is shown in Figure 2a. A dual channel analog reformatting memory allows in-phase (I) and quadrature (Q) video components from a coherent radar to be used in conjunction with a complex CZT processor in order to preserve the sense of the doppler

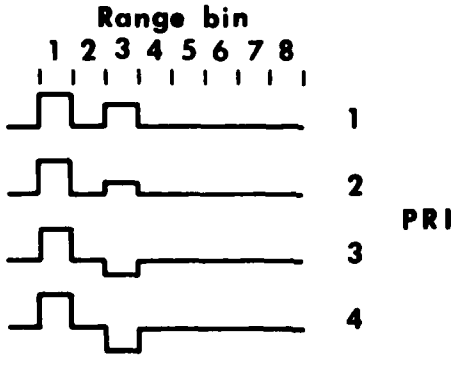


a) TRANSMITTER PULSE WAVEFORM

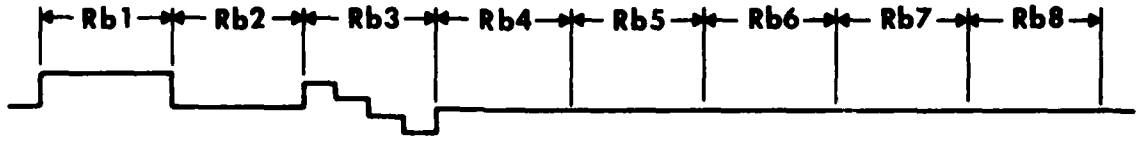
b) RAW VIDEO



c) FILTERED AND SAMPLED VIDEO



d) VIDEO IN MATRIX FORMAT



e) REFORMATTED VIDEO

Figure 1. Video Reformatting in Radar Doppler Processor

information (approaching vs. receeding targets). One aspect which is particularly crucial in the complex doppler processor involves gain tracking between the I and Q reformatting memories. In order to ensure that the doppler image response (having doppler sense opposite that of the target) is sufficiently attenuated, the gain between I and Q channels must continually track to within limits given by

$$20 \log_{10}\left[\frac{A_I + A_Q}{|A_I - A_Q|}\right] > DR \tag{1}$$

where DR is the desired processor dynamic range in dB.

Two additional processor architectures are illustrated in Figure 2 which use an MxN reformatting memory to expand the capabilities of the chirp Z-transform and the digital-analog correlator. Figure 2b illustrates the use of the MxN reformatting memory between N-point and M-point chirp Z-transform processors to perform the analog two dimensional discrete Fourier transform (DFT) of an MxN element array. The DFT of a finite area sequence f(m,n) is

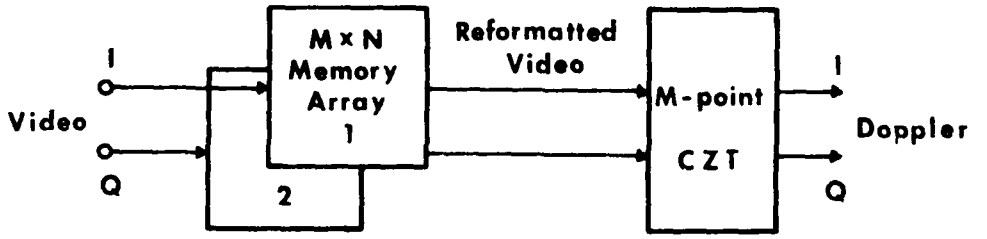
$$F(k,\ell) = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} f(m,n) \exp\left[-j2\pi\left(\frac{km}{M} + \frac{\ell n}{N}\right)\right] \tag{2}$$

The two dimensional DFT can be interpreted in terms of the one dimensional DFT by expressing the above as

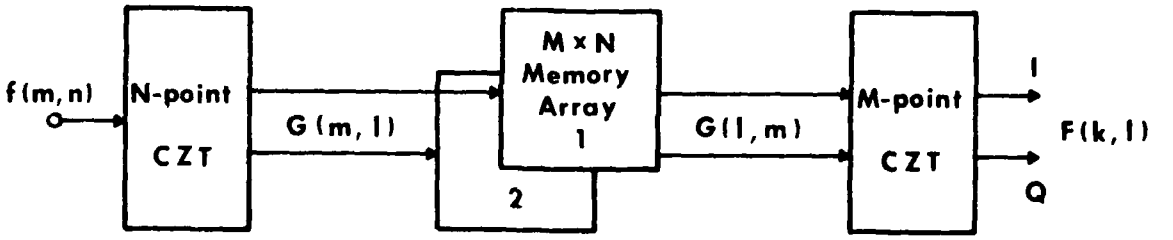
$$F(k,\ell) = \sum_{m=0}^{M-1} G(m,\ell) \exp\left(-j2\pi \frac{km}{M}\right) \tag{3}$$

where

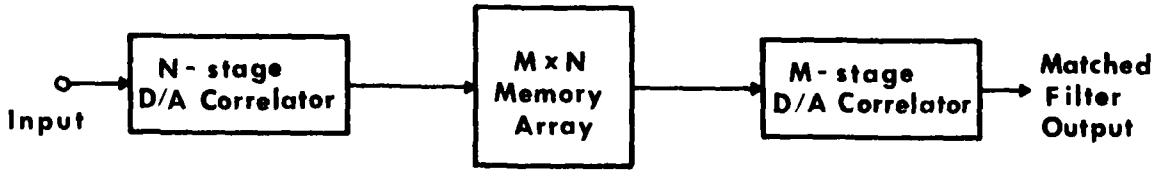
$$G(m,\ell) = \sum_{n=0}^{N-1} f(m,n) \exp\left(-j2\pi \frac{\ell n}{N}\right) \tag{4}$$



a) DOPPLER PROCESSOR



b) TWO-DIMENSIONAL CZT



c) MN-STAGE PROGRAMMABLE MATCHED FILTER

Figure 2. CCD Analog Signal Processor Architectures

$G(m,\ell)$ corresponds to an N-point one dimensional DFT for each value of m, i.e., it consists of M one dimenstional transforms, one for each row of $f(m,n)$. The two dimensional DFT $F(k,\ell)$ is then obtained by performing N one dimensional transforms on the reformatted columns of the sequence $G(m,\ell)$.

In Figure 2c the CZT processors have been replaced with M-stage and N-stage digital-analog correlators, resulting in a fully programmable matched filter having MN stages. The approach is based on a signaling waveform consisting of a code withing a code, as illustrated in Figure 3. The inner code (S_1) is shown as a triangular waveform and the outer code (S_2) is a binary pseudorandom sequence but both are, in general, arbitrary waveforms determined by the digital references in the digital-analog correlators. The time-bandwidth product of the processor is MN.

As is seen in Figure 2, an analog reformatting memory represents another important building block in the CCD signal processing repertoire which expands the capabilities of the CZT and digital-analog correlator devices. This paper describes the development of an analog reformatting memory which employs two-dimensional charge transfer cells in order to achieve high performance and maintain dynamic range.

II. ALTERNATIVE MEMORY ARCHITECTURES

Analog CCD reformatting memories have been recently applied in high speed doppler processors in conjunction with surface acoustic wave device chirp transform processors.[3-6] These memories are predominately line-addressed CCD structures utilizing N delay lines each having M stages. A typical configuration is shown in Figure 4, again using the 4x8 format as an example. The individual CCD input and output circuits are commutated, usually by means of on-chip MOS circuitry.

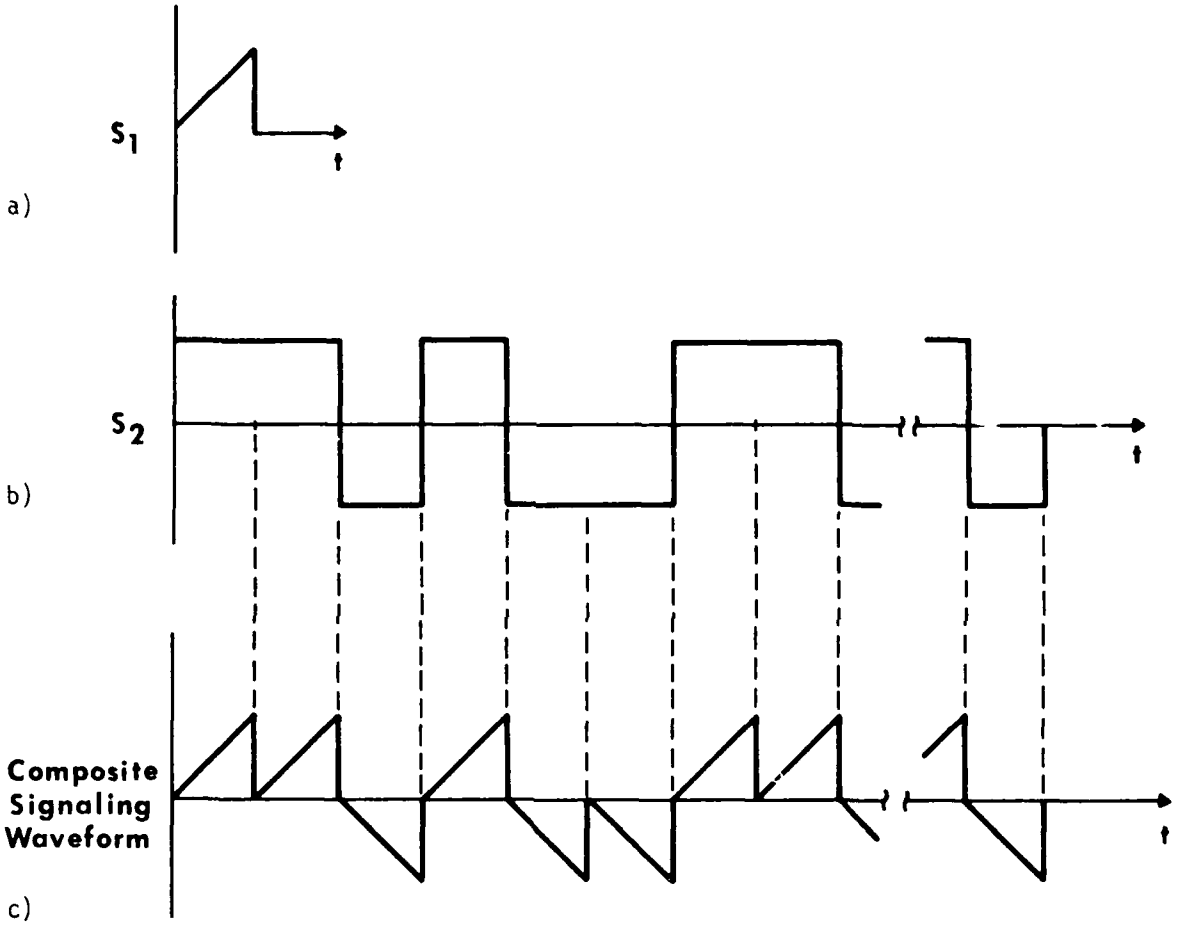


Figure 3. Signalling Waveform in the Matched Filter
a) Inner Code, b) Outer Code, c) Composite

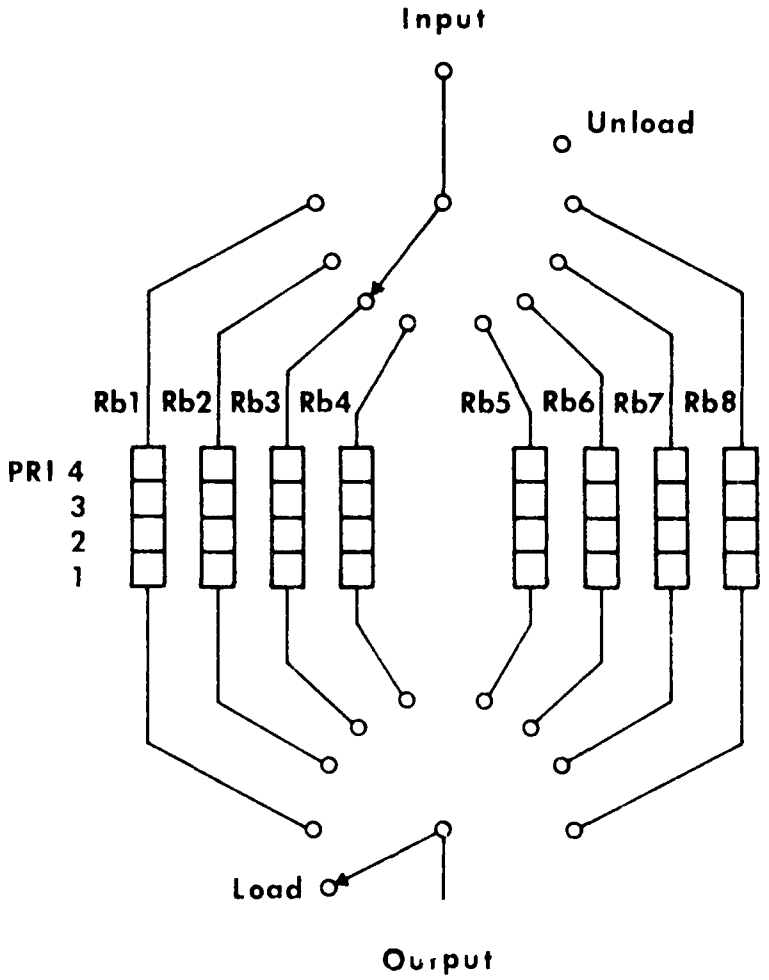


Figure 4. Line Addressed Reformatting Memory Organization

The memory is loaded in a row-by-row fashion by commutating the input circuit, at the desired sampling rate. After each row has been entered, it is transferred one stage toward the output. When the memory is filled, delay line 1 contains the samples from range bin 1, delay line 2 contains those from range bin 2, etc. Reformatting is accomplished by emptying the array column-by-column using the output commutator. Since data cannot generally be entered during this output phase, the duty cycle of this configuration is limited to 50%.

Note that the inverse operation is possible in square arrays, in which data can be entered column-by-column during the output phase of one reformatting operation, then emptied row-by-row during the input phase of the next. This specific case results in 100% duty cycle, however, the key limitation in the CCD delay line approach is the fixed pattern gain and offset variations that occur among the delay lines due to MOS threshold voltage variations and, to a lesser extent, CTE variations.[6] In the doppler processor application, these result in gain and offset variations among the length M output records in the column-output mode, and among samples in each record in the row-output mode. The former may be tolerated in some applications, however, the latter usually results in an intolerable signal to noise degradation. In the case of the 2-dimensional CZT and the MN stage matched filter, both effects contribute to degradation of dynamic range.

Since the reformatting operation consists in interchanging row and column transfer of the stored data sequence, the most direct realization of a CCD reformatting memory involves a structure in which charge can be transferred either vertically (row-by-row) or horizontally (column-by-column) in the array.[7] The structures controlling the two dimensional charge transfer operation are complicated, and the potential advantages of this direct realization are lost in the higher risks associated with the sophisticated design. In addition, there

is no performance advantage over line addressed structures if individual input and output cells are employed at the edge of the array. However, the two dimensional transfer approach offers the potential for substantially improved performance with the integration of a CCD multiplexer and demultiplexer to provide serial interfaces with the memory array. A block diagram of the structure appears in Figure 5. The input demultiplexer performs a serial-to-parallel conversion and loads the memory array row-by-row. During the load cycle charge is transferred vertically in the array. When all rows have been loaded, the array is switched to a horizontal transfer mode and the output multiplexer performs the required parallel-to-serial conversion of the data stored in each column. The resulting CCD structure has a single input port (voltage-charge conversion) and a single output port (charge-voltage conversion). All intermediate data manipulations involve CCD-type charge transfers. Thus, the sources of the fixed pattern variations which cause degraded dynamic range in the line - addressed structures have been eliminated and there is potential for thermal noise limited dynamic range over the entire reformatted data array (MN samples).

In square arrays (M=N) an additional demultiplexer can be added at the left of the memory array in Figure 5, and an additional multiplexer added at the bottom to allow simultaneous loading and unloading. Full duty cycle is thereby achieved and, in addition, the array can be operated as a serial-parallel-serial (SPS) delay line. The latter feature greatly simplifies device evaluation.

III. MEMORY ARRAY DESIGN

Because of the potential for greatly expanded signal processing capabilities, and based on previous experience with line-addressed structures,[5] a development program was initiated to design an analog CCD reformatting memory using the two-dimensional charge transfer approach. The specifications chosen for the prototype memory include a 32x32 element array size, dynamic range greater than

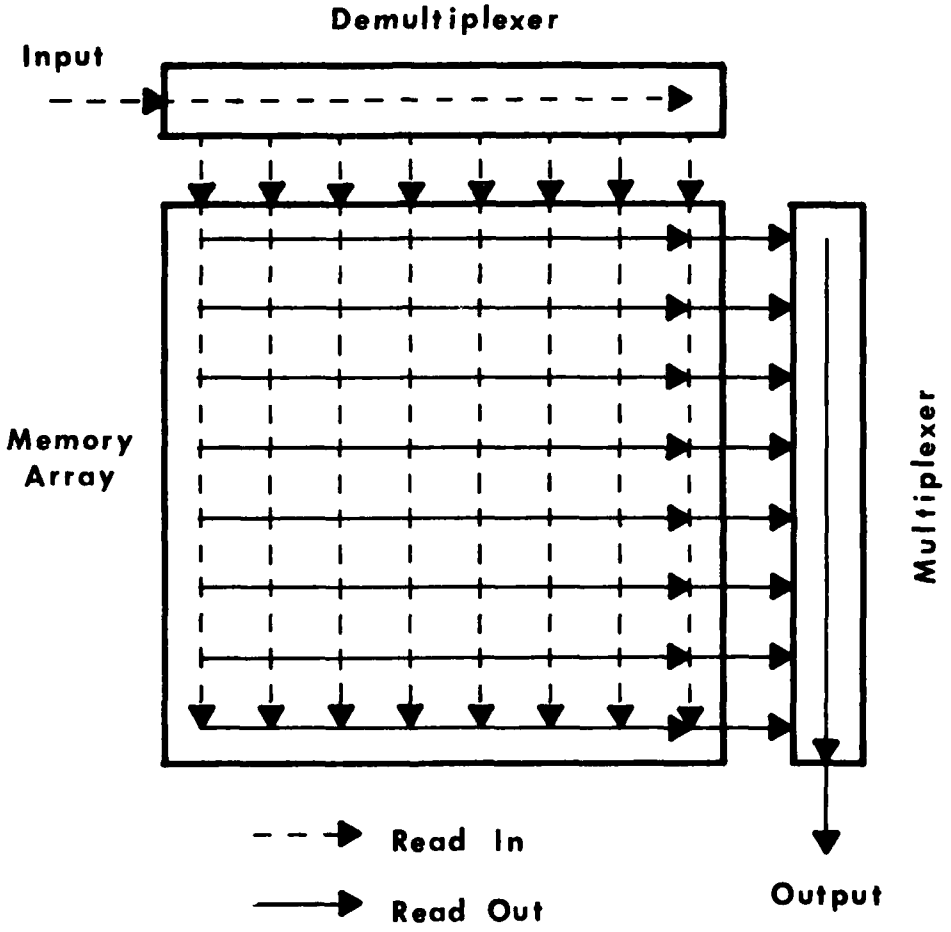


Figure 5. Organization of the Two-Dimensional Reformatting Memory

40 dB, high speed operational capabilities and compatibility with the current double-level self-aligned polysilicon gate process. This process includes self aligned well implants to allow fabrication of two-phase CCDs.

The key design consideration is mating the multiplexer and demultiplexer structures to the two dimensional transfer cells. Sequin[7] has shown that at least three independent electrode systems are required to accomplish two dimensional charge transfer. In addition, he has developed a diagonally connected electrode scheme which is compatible with two-level gate structures and requires no interlevel contacts inside the array. Unfortunately, the clocking scheme and the structure of this optimal architecture make the multiplexer and demultiplexer designs extremely complex. In order to simplify these critical interfaces, a more straightforward two dimensional cell design was adopted which relies on interlevel interconnects within the array. The structure is similar to a 3-gate level design discussed by Sequin [Ref. 7, Figure. 5b], and is shown pictorially in Figure 6. The cell consists of two interleaved two-phase CCDs which share a common phase. The V and H transfer gates are both first level polysilicon electrodes. The H gates are continuous polysilicon in the vertical direction, and columns are interconnected with metal. The V gates rely solely on metal interconnects. The common phase is second level polysilicon which completely covers the array except for the openings required for contact to the first level gates. Figure 7 is a photomicrograph showing the important features of the two dimensional transfer cell. The cell dimenstions are 2.0 mils x 2.0 mils and are dictated by the minimum intralevel gate spacing and charge capacity considerations. The interconnects are redundant to provide a measure of protection against a few open metal lines.

The demultiplexer and multiplexer structures were realized as 4-phase devices having 0.5 mil gate lengths in order to match the two dimensional cell spacing. Channel and gate levels of the demultiplexer are illustrated in Figure 8. The

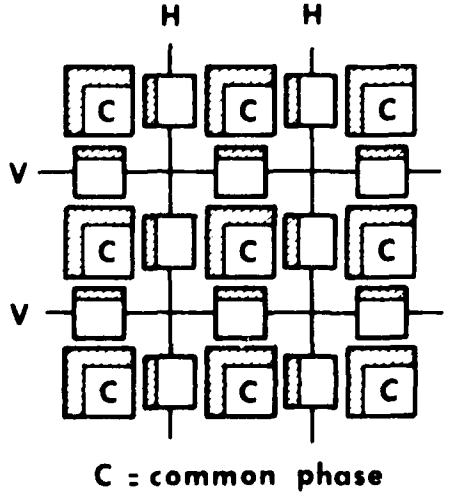


Figure 6. Representation of the Two-Dimensional Charge Transfer Cell

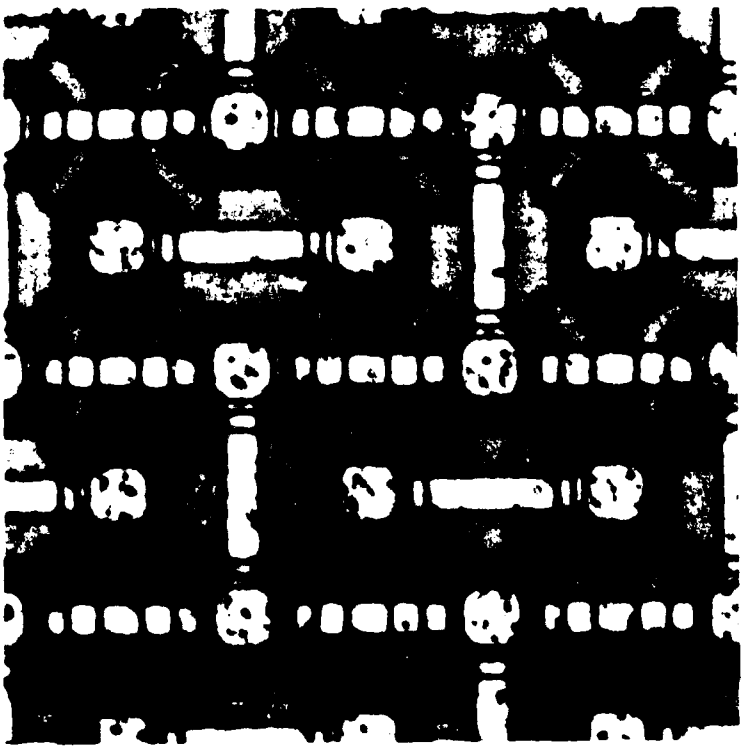


Figure 7. Photomicrograph of the Two-Dimensional Transfer Cell

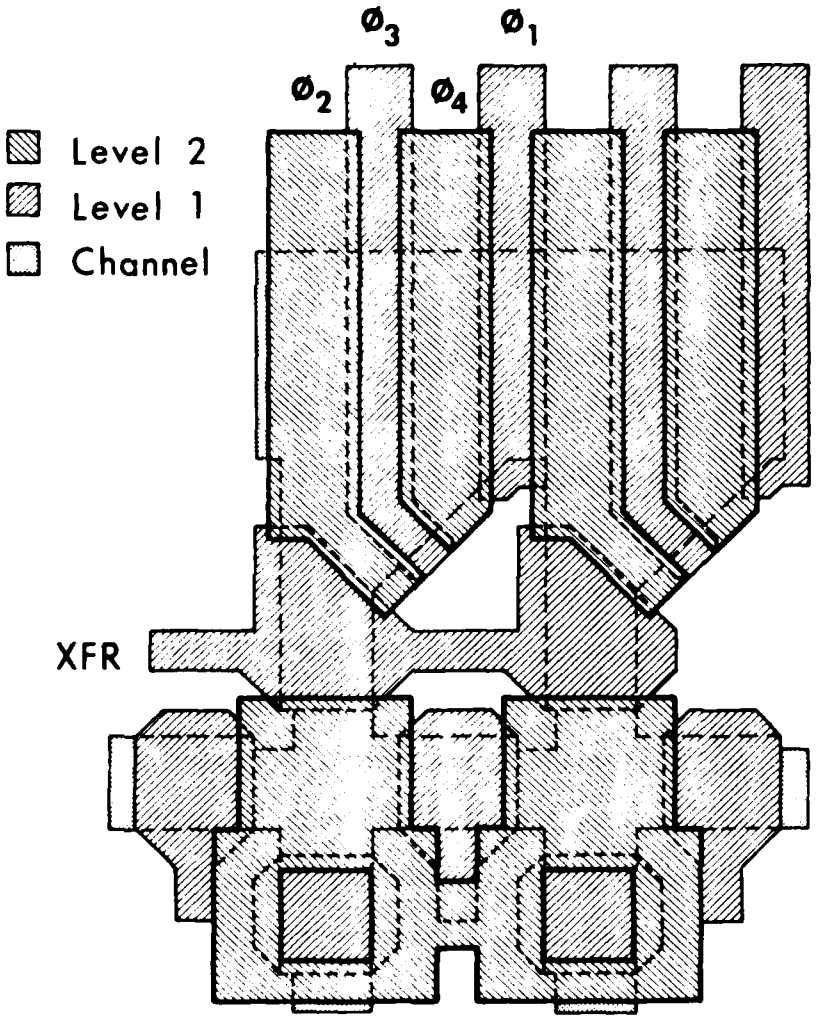


Figure 8. Channel and Gate Levels of the Demultiplexer Structure

parallel transfer is accomplished by inhibiting the ϕ_3 clock and enabling the XFR gate. Charge stored beneath the ϕ_2 electrode is then transferred to the XFR gate and subsequently to the second level gate in the two dimensional transfer cell. The interface between the ϕ_2 and XFR electrodes is slanted to provide increased gate width and to minimize charge trapping in the demultiplexer which could degrade CTE during the serial load operation. A photomicrograph showing the demultiplexer - memory array interface appears in Figure 9. Note that incomplete charge transfer in the parallel transfer operation results only in an apparent attenuation of the signal, so long as the charge remaining in the demultiplexer is completely cleared during the subsequent load operation.

The channel and gate levels of the multiplexer structure are illustrated in Figure 10. The parallel transfer is accomplished between an extended second level memory array electrode and the ϕ_2 multiplexer gate by means of a short first level transfer gate. As in the demultiplexer, the interface is slanted to provide maximum channel width. An individual drain diode is included in each multiplexer cell and is connected to the extended output electrode by means of a short tab added to the adjacent first level memory array gate. This arrangement ensures clearing of any residual charge following the parallel transfer which would otherwise degrade the apparent CTE of the memory array. A photomicrograph showing the multiplexer - memory array interface appears in Figure 11.

Figure 12 is a photomicrograph of the complete 32x32 element memory. The entire structure is buried channel, with the exception of the demultiplexer input circuitry which is surface channel. The multiplexer channels are joined in a common output diode and charge sensing is accomplished with a standard reset amplifier configuration. The die dimensions are 112.5 mils x 114 mils.

IV. EXPERIMENTAL RESULTS

Successful operation of the memory has been achieved at clock rates exceeding

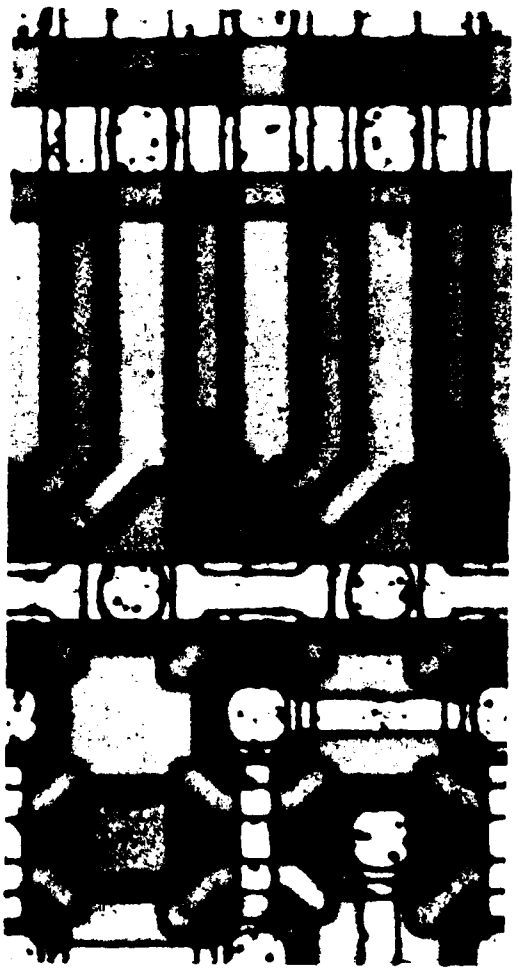


Figure 9. Photomicrograph of the Demultiplexer - Memory Array Interface

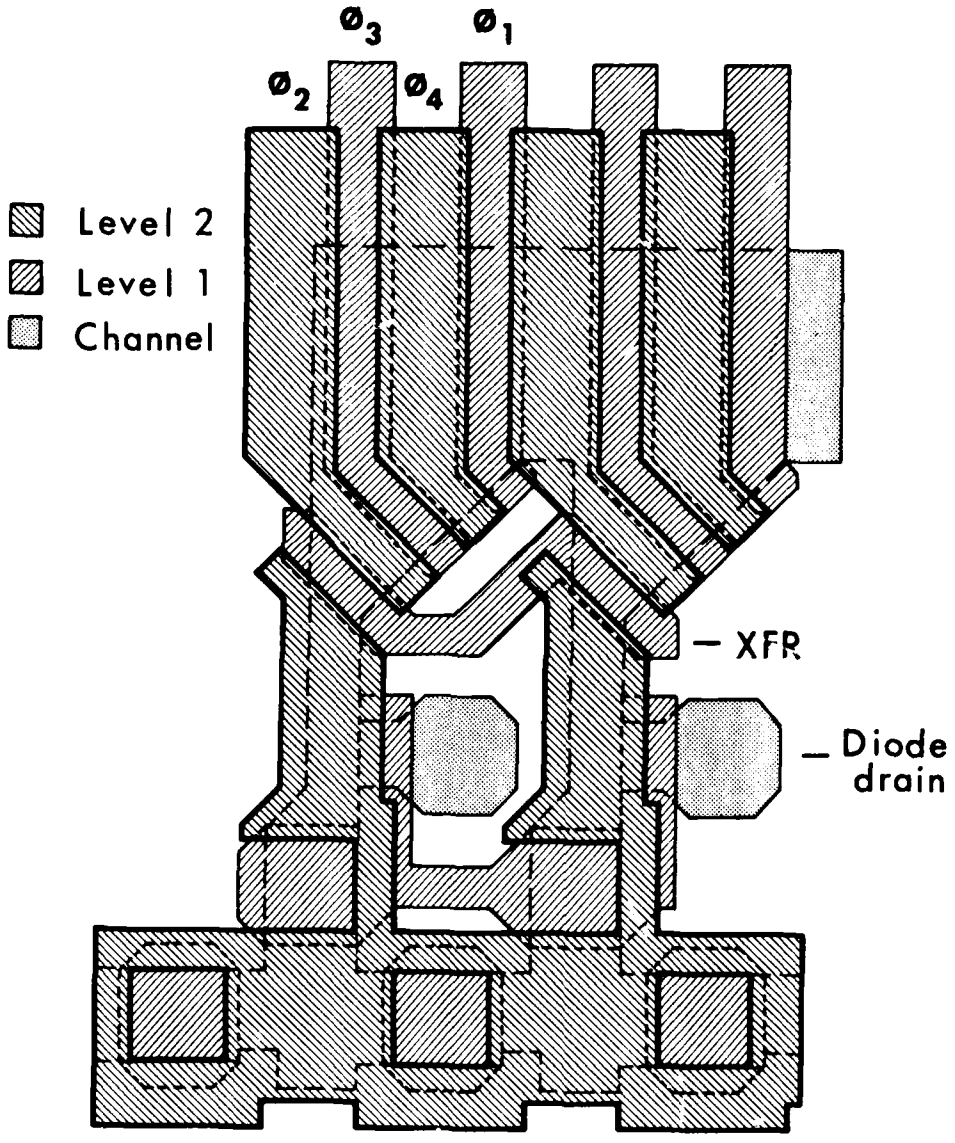


Figure 10. Channel and Gate Levels of the Multiplexer

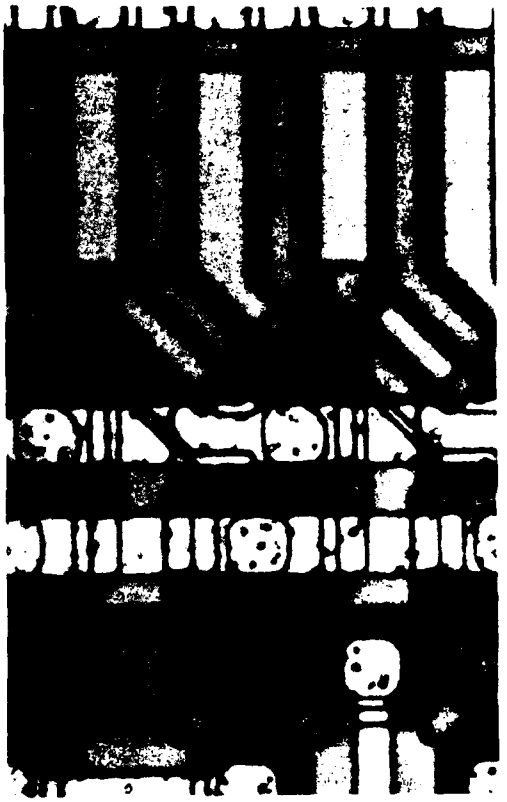


Figure 11. Photomicrograph of the Multiplexer - Memory Array Interface

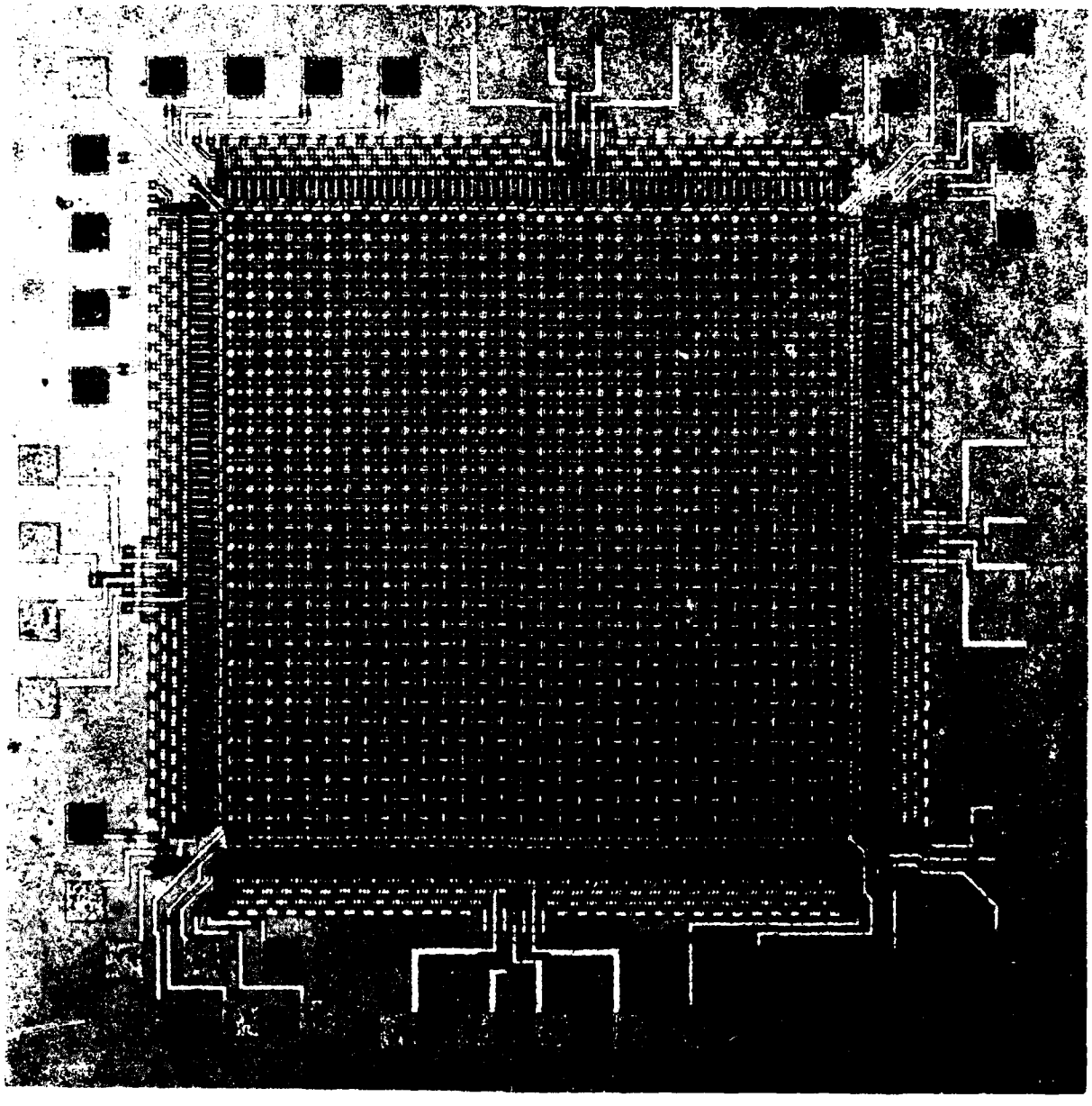


Figure 12. Photomicrograph of the 32 x 32 Element Reformatting Memory Chip

5 MHz. This upper limit is presently dictated by the test circuitry used to generate the 15 clock waveforms necessary for 100% duty cycle operation. Figure 13 shows input and output waveforms for memory operation at 1 MHz in the SPS mode, corresponding to a 1024 stage shift register. Charge transfer efficiency (CTE) has been computed from the observed step response in this mode (assuming that it is dominated by demultiplexer and multiplexer transfers) and is greater than 0.9999 at 1 MHz.

Operation in the reformatting mode with 100% duty cycle at a 1 MHz rate is illustrated in Figure 14. Figure 14a shows the test waveform which is triggered once per frame (1024 cycles). Figure 14b shows memory output over two successive frames and demonstrates the full duty cycle capabilities. Figure 14c and d are expanded views of the output during the first frame and confirm the reformatting operation which, in this case, corresponds to a 32x time compression of the test waveform.

Figure 15 shows the memory output on a more sensitive scale with a dc input signal and illustrates that, although fixed pattern noise has been dramatically reduced (as compared to line addressed arrays) it has yet to be eliminated. Figure 15a corresponds with Figure 14b and shows a line-to-line fixed pattern offset distribution having an RMS value which is approximately 43 dB below the maximum peak to peak signal illustrated in Figure 14.

Figure 15b corresponds with Figure 14b and indicates excellent fixed pattern noise performance within each line (32 samples). A slight upward tilting of the waveform can be discerned which is due to a leakage current component. The tilt is caused by the fact that each consecutive sample in a line was stored in the two-dimensional array for one additional cycle.

The lack of an appreciable fixed pattern component in Figure 15b indicates that the component observed in Figure 15a is added in the input demultiplexers. It is currently believed that this component is caused by spatial variations in the surface potential beneath the ϕ_2 demultiplexer clock electrode which result in

a)

b)

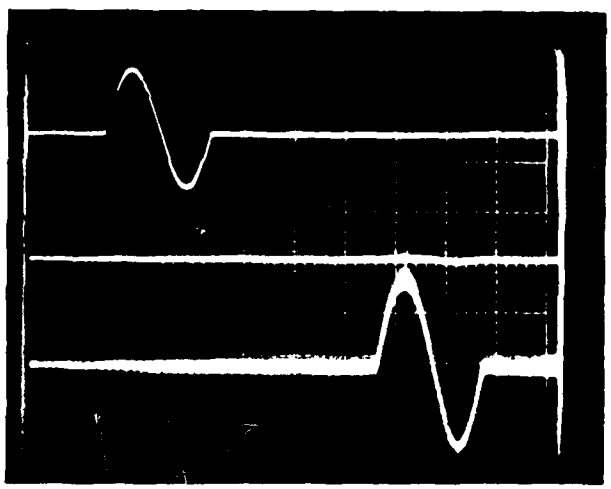


Figure 13. SPS Operation of the Memory at 1 MHz. a) Input Waveforms, 0.5V/div, b) Memory Output, 0.05V/div. Horizontal scale 200 μs/div

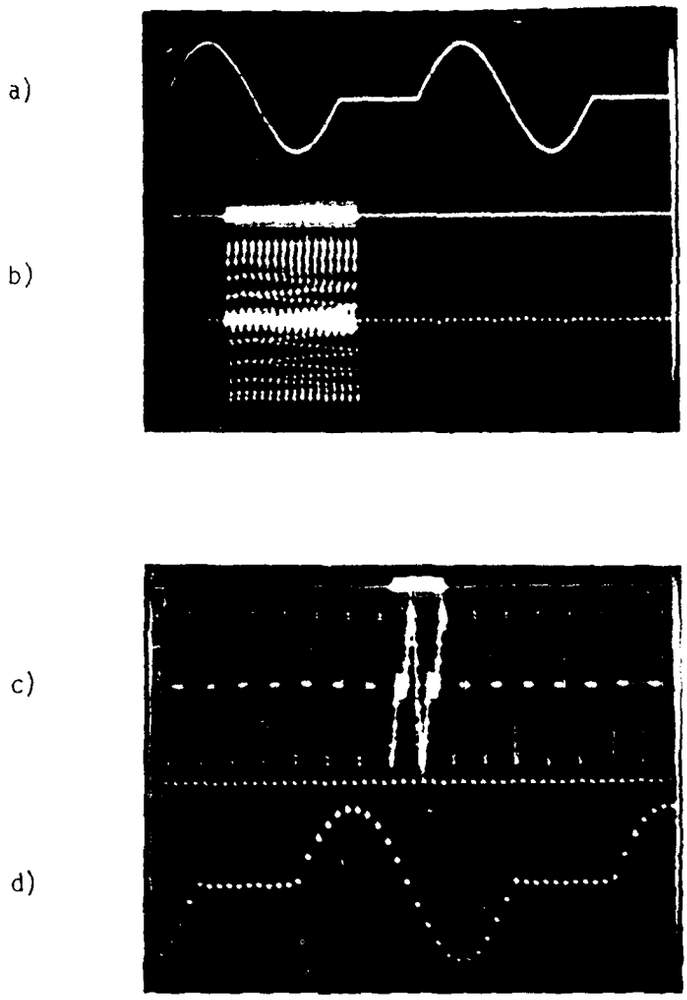
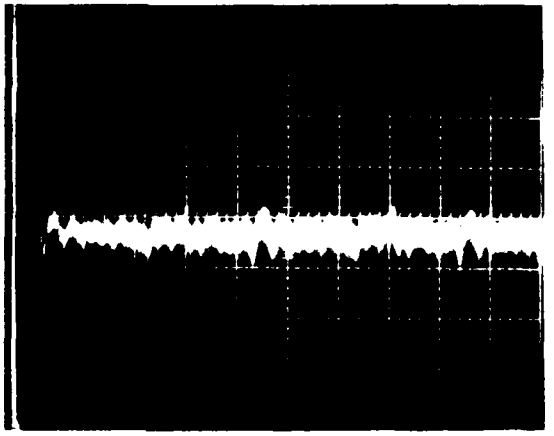


Figure 14. Reformatting Operation of the Memory at 1 MHz. a) Input Waveform, 0.5V/div, b) Memory Output 0.05V/div. Horizontal Scale 200 μs/div. c) Memory Output, 50 μs/div, d) Memory Output 5 μs/div.

a)



b)

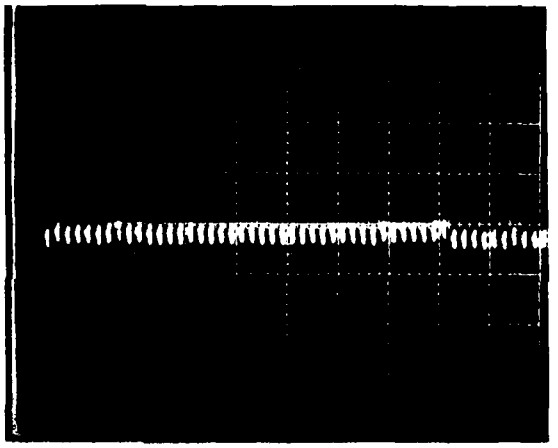


Figure 15. DC Response in Reformatting Mode Showing Fixed Pattern Noise Components. a) Frame to Frame, 5 mV/div, 500 µs/div, b) Line to Line, 5 mV/div, 5 µs/div.

incomplete charge transfer into the memory array. (See Figure 8.) These variations can be caused by localized variations in substrated doping or surface state density, and further work is in progress to minimize them.

V. APPLICATION EXAMPLE

In order to demonstrate the application of the reformatting memory in analog signal processors, a breadboard version of the doppler processor shown in Figure 2a has been constructed. This subsystem uses two of the 32x32 memory arrays and an integrated 32 point CZT processor chip. The I and Q output signals from the CZT are squared and summed to provide the power density spectrum of a synthetic radar signal obtained from a specially constructed simulator. This simulator provides two phase coherent signals at 32 doppler frequencies which may independently occur in any of 100 available range bins. Because a full complex CZT is utilized, the maximum duty cycle is limited to 50%. A special memory timing circuit was constructed which permits synchronization of the memory and CZT with the simulator.

Figures 16, 17 and 18 illustrate the operation of the doppler processor. For these tests a clock rate of 100 KHz was utilized, resulting in a 1 ms PRI in the simulator. Figure 16 shows the simulator output with doppler signals inserted in range bins 5 and 25. The doppler rates are not indicated in the figure, however, they were adjusted to correspond to doppler bin 27 (843.75 Hz) in range bin 5 and doppler bin 5 (156.25 Hz) in range bin 25. Figures 17 (a-c) show the output from I and Q memories and the CZT for 1 frame (32 PRIs). The intensified portion of the traces are shown in Figure 17 (d-f) and correspond to range bins 0 through 9. The reformatted doppler signal can be observed in range bin 5, as can the single output sample from the CZT during the corresponding transform interval. Note the appreciable slope in the memory output waveforms in adjacent range bins caused by integration of leakage current over the long

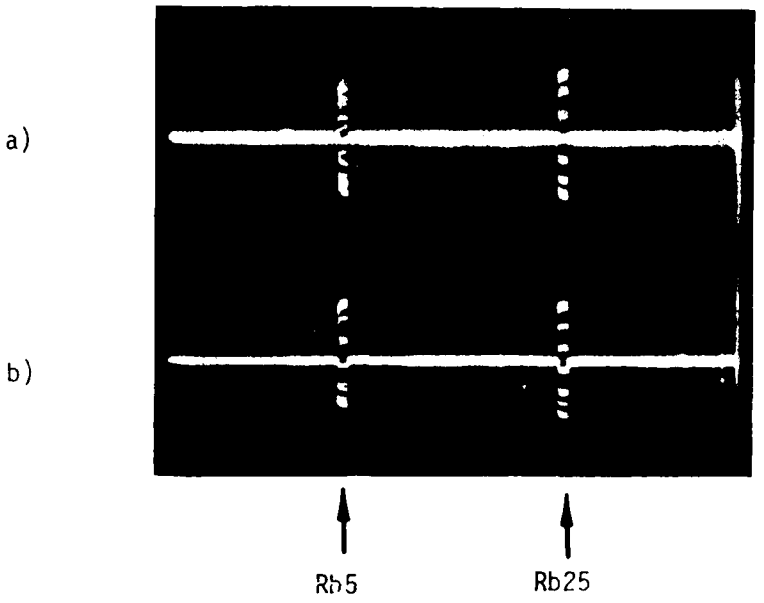


Figure 16. Radar Simulator Output Waveforms
a) In Phase component, b) Quadrature Component

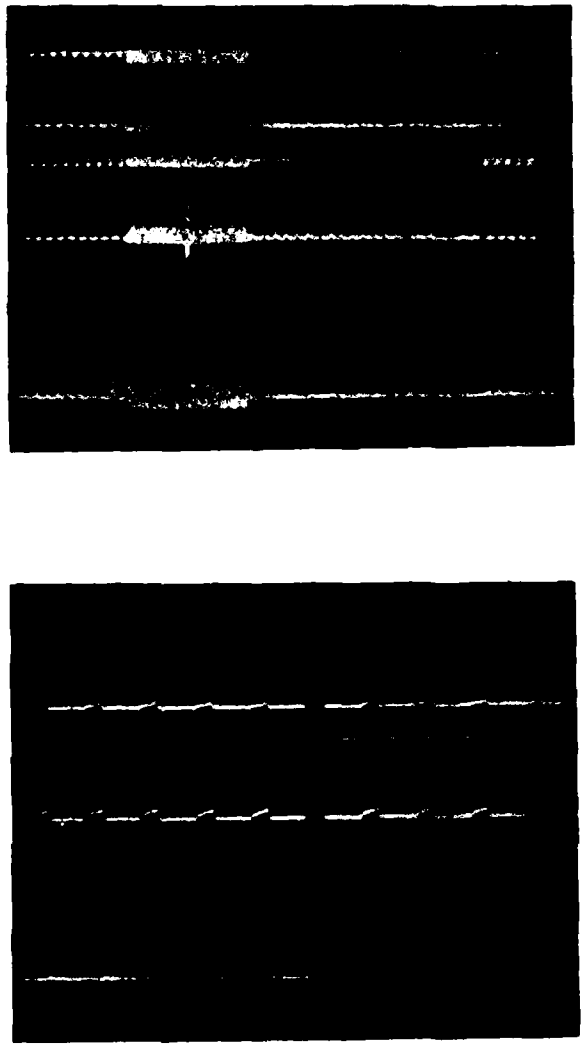
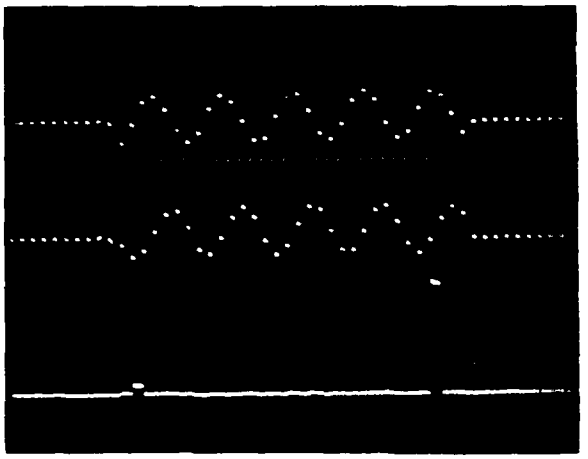


Figure 17. Memory and CZT Output Waveforms. a) Memory I Output, 1V/div, b) Memory Q Output, 1V/div, c) CZT Output 0.5V/div. Horizontal Scale 5 ms/div. d), e), and f) Show Intensified Portion of Top Photograph, Horizontal Scale 1 ms/div.

a)



b)

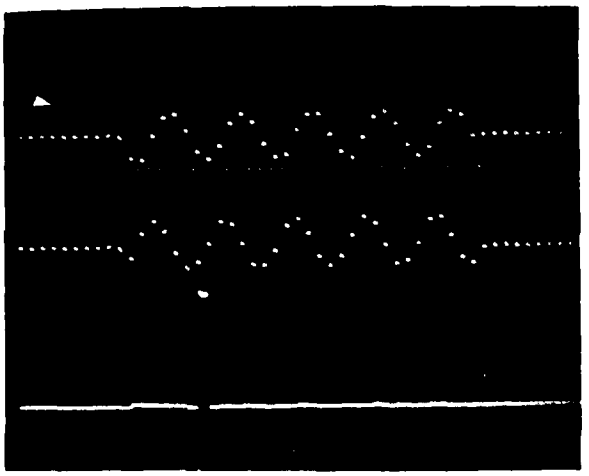


Figure 18. Detailed Memory and CZT Output Waveforms
a) Range bin 5, b) Range bin 25.
Horizontal Scale 500 μs/div.

(32 ms) frame interval.

Figure 18a shows details of the memory and CZT output waveforms in range bin 5. Due to an error in coding CCD filter tap weights on the CZT chip, the sequence of doppler bins is 31, 0, 1, 2,..., 30. A small dc offset marks doppler bin 0, and the doppler signal is found to occur, as expected, in bin 27. Figure 18b shows identical waveforms for range bin 25, and the doppler output from the CZT is seen in bin 5. In figure 18a and 18b the memory waveforms appear to be the same because of aligning, however, the phase information has been preserved resulting in the proper frequency output from the CZT. The dynamic range of the CZT chip is 50 dB, although this is reduced by the external analog multipliers used to obtain the power density spectrum shown in the figures.

The circuitry included in these preliminary tests occupies a volume of approximately .06 cu.ft. and dissipates about 5.7 watts. A considerable reduction in power dissipation can be obtained by more complete integration of the support circuitry required by the memory chips.

Preliminary results from a breadboard version of the two-dimensional CZT circuit shown in Figure 2b have been presented elsewhere.[8] This circuit is being evaluated for signal processing applications, and more detailed performance results will be presented at a later date.

VI. CONCLUSIONS

The design of a high performance, low noise analog CCD reformatting memory has been described which utilizes two dimensional charge transfer. This unit has been shown to be an important addition to the growing list of CCD signal processing circuits which expands the capabilities of units such as the chirp Z-transform and digital-analog correlator. Although dynamic range is currently limited by fixed pattern offsets which are apparently generated at the demultiplexer-memory array interface, the observed performance is vastly superior to that seen in line-addressed versions.

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